

ABSTRACT OF THE DISCLOSURE

Arbitration of Data Transfer Requests

A data processor core 10 comprising: a memory access interface portion 30
5 operable to perform data transfer operations between an external data source and at
least one memory 120 associated with said data processor core; a data processing
portion 12 operable to perform data processing operations; a read/write port 40
operable to transfer data from said processor core to at least two buses 75A, 75B said
at least two buses being operable to provide data communication between said
10 processor core 10 and said at least one memory 120, said at least one memory 120
comprising at least two portions 120A, 120B, each of said at least two buses 75A, 75B
being operable to provide data access to respective ones of said at least two portions
120A, 120B; arbitration logic 110 associated with said read/write port 40; wherein said
arbitration logic is operable to route a data access request requesting access of data in
15 one portion of said at least one memory received from said memory access interface to
one of said at least two buses providing access to said one portion of said at least one
memory and to route a further data access request requesting access of data in a further
portion of said at least one memory received from said data processing portion to a
further one of said at least two buses providing access to said further portion of said at
20 least one memory, said routing of said data access requests being performed during the
same clock cycle.

Fig 5